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Original Research Paper

Design of Coherent Envelope Measurement Circuit Based on Direct Digital Frequency Synthesizer

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Abstract: Envelope detection and measurement has important applications in many domains such as instrumentation, sensors characterization, analog and digital communications. Instead of other envelope detection methods that use analog circuits or digital filters, we propose an electronic circuit that operates measurement in coherent mode. After reproduction of the input wave frequency using direct digital synthesizer, we place the envelope on a new low reference frequency signal followed by an analog measurement block based on analog multipliers and low-pass filters. Design circuit, simulation and experimental results are presented to validate the measurement for different values of input and reference frequencies.

Keywords: *Analog filter, Analog multiplier, Coherent mode, Direct digital synthesis, Envelope.*

1. Introduction

In many applications, the envelope of received or analyzed signal contains the required information to characterize sensors or systems such as quartz crystal biosensors [1], RFID communications [2], photonic and fibre transmission [3]. Among the most used techniques, there are analog basic circuit using electronic components (diode, resistor, and capacitor) and a squaring low-pass filtering where the envelope detection involves squaring the input signal and sending this signal through a low-pass filter. Further, the digital envelope detection method involves creating the analytic signal of the input using the Hilbert transform. For synchronous mode, the phase-locked loop (PLL) has been exploited to produce the envelope of received signal in accordance to the frequency [4][7-10]. However, these methods have two disadvantages: nonlinearities of square root block and non-coherent detection when the frequency of input wave changes [5]. To overcome these drawbacks, we propose a new circuit that operates in coherent mode without any nonlinear operations. Coherent mode means that the circuit detects the input fundamental frequency and reproduces a low reference frequency with the same envelope to be measured. To this end, we use the Direct Digital Synthesis (DDS) method whose principle is recalled below.

1.1. Inputs/outputs of the measurement circuit

The proposed circuit shown in Fig.1, transforms the envelope of the input wave on the reference signal where the frequency is numerically controlled. After the transformation block, the envelope is measured by a multiplier and low-pass filter.

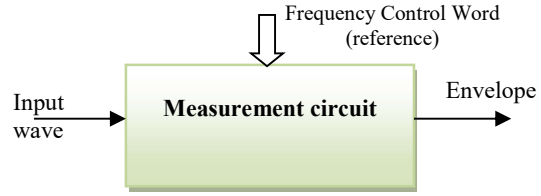

Figure 1. Inputs/outputs of a DDS based envelope measurement circuit

1.2. DDS principle

The aim of direct digital synthesizers (DDS) is to synthesize sine waves using digital technique with high precision and low frequency tuning [6]. The conventional architecture of DDS circuit is shown in Fig.2; whose components are:

- *Phase Accumulator:* provides the time reference of the wave form stored in the memory address for reading the instantaneous values.
- *Waveform Memory*: contains samples of the waveform to be synthesized.
- *D/A Converter*: converts each digital value into its proportional analog voltage.
- *Low-pass Filter:* limits the spectrum of the synthesized wave at the Nyquist bandwidth related to the operating clock frequency F_{CLK}.

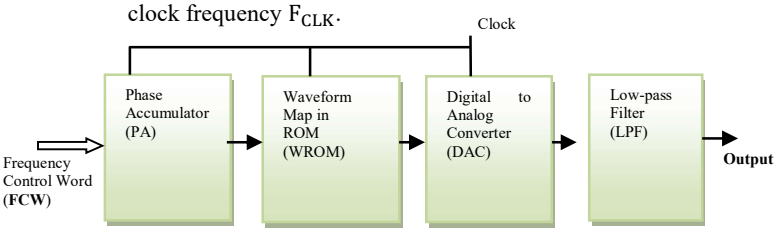

Figure 2. Conventional architecture of DDS

The output frequency F_{OUT} depends on the reference clock frequency F_{CLK}, the frequency control word FCW and the size of the phase accumulator N, by the following expression.

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$$F_{OUT} = \frac{FCW}{2^N} F_{CLK} \quad (1)$$

This paper is organized as follows. In section 2, we present the architecture and coherent measurement technique. Simulink implementation and simulation results are illustrated in section 3. Finally, experimental results are presented and discussed in section 4.

2. Architecture of Circuit and Coherent Detection Method

The architecture of the proposed envelope coherent detection circuit based on DDS technology is shown in Fig.3. The input wave corresponds to a sine signal modulated by the low frequency envelope $m(t)$ according to the expression: $v_I(t) = V_I(1 + m(t)) \sin(2\pi f_I t)$.

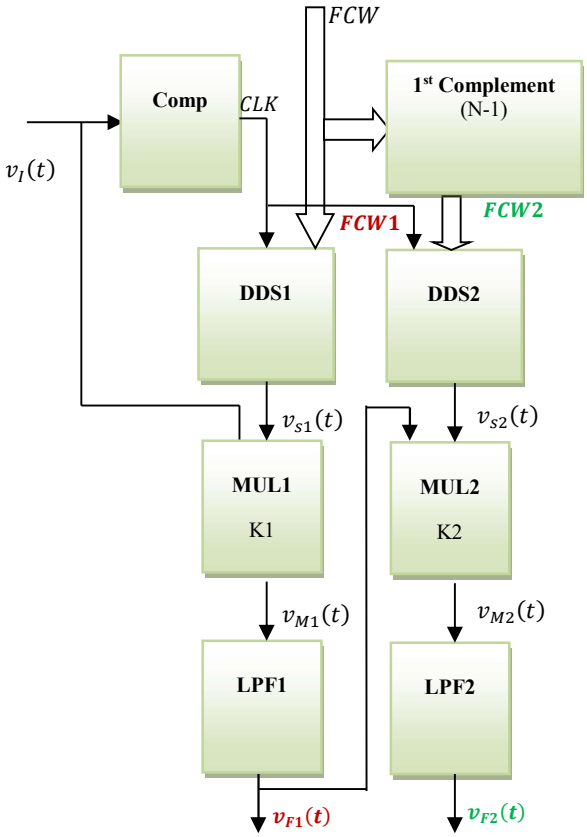

Figure 3. Block diagram of coherent envelope detection circuit based DDS

The proposed circuit has the following blocks:

- *Comparator:* the comparator transforms the input wave to logic signal CLK with falling and rising edges. This signal represents a synchronization clock of DDS blocks.

- *DDS blocks*: DDS blocks (DDS1 and DDS2) are triggered on rising and falling edges of comparator. As shown in Fig.4, the phase accumulators are updated according to $\frac{T_I}{2}$ period and consequently the DDS outputs take the following expressions:

$$f_{s1} = 2 \times \frac{FCW}{2^N} F_I \quad (2)$$

$$f_{s2} = 2 \times \frac{2^{N-1} - FCW}{2^N} F_I \quad (3)$$

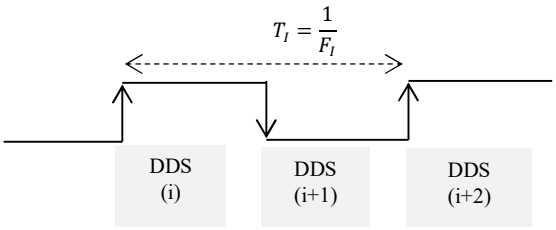

Figure 4. Output of comparator and DDS timing activation

Therefore, the waves of DDS blocks are expressed as:
$v_{s1}(t) = V_{s1} \sin(2\pi f_{s1} t + \varphi_{s1})$; $v_{s2}(t) = V_{s2} \sin(2\pi f_{s2} t + \varphi_{s2})$

- *Reference block*: the reference block aims to translate the input wave to another wave with the same envelope but with low reference frequency F_0. It is composed of Multiplier MUL1 and Low-pass filter LPF1 whose produced signal is expressed as:

$$\begin{aligned} v_{M1}(t) &= K_1 v_{s1}(t) v_I(t) \\ &= \frac{K_1 V_{s1} V_I}{2}(1 + m(t))(\cos(2\pi(f_I - f_{s1})t - \varphi_{s1}) \\ &\quad - \cos(2\pi(f_{s1} + f_I)t + \varphi_{s1})) \end{aligned} \quad (4)$$

After low-pass filter, the high frequency component $f_{s1} + f_I$ will be more attenuated and the signal $v_{F1}(t)$ is written as,

$$v_{F1}(t) = \frac{K_1 V_{s1} V_I}{2}(1 + m(t))(\cos(2\pi F_0 t + \varphi_{s1}) \quad (5)$$

where:

$$\begin{aligned} F_0 &= f_I - f_{s1} \\ &= (1 - \frac{FCW}{2^{N-1}}) \times F_I \end{aligned} \quad (6)$$

- *Detection block:* the detection block composed of multiplier MUL2 and Low-pass filter LPF2 aims to produce the envelope $V_I(1 + m(t))$ according to the following equations,

$$\begin{aligned} v_{M2}(t) &= K_2 v_{s2}(t) v_{F1}(t) \\ &= \frac{K_1 K_2 V_{s1} V_{s2} V_I}{2}(1 + m(t)) \cos(2\pi F_0 t + \varphi_{s1}) \times \sin(2\pi F_0 t + \varphi_{s2}) \\ &= \frac{K_1 K_2 V_{s1} V_{s2} V_I}{4}(1 + m(t))\,(\sin(\varphi_{s2} - \varphi_{s1}) + \sin(4\pi F_0 t + \varphi_{s1} + \varphi_{s2}))) \end{aligned} \quad (7)$$

$$v_{F2}(t) = \frac{K_1 K_2 V_{s1} V_{s2} V_I}{4}(1 + m(t)) \sin(\varphi_{s2} - \varphi_{s1}) \quad (8)$$

3. Simulink Design and Simulations

3.1. Simulink Design

The Matlab-Simulink design of the proposed circuit is shown in Fig. 5. The required components are given as follows:

- *Comparator*: it transforms analog input wave to logic signal that represent the clock of DDS.
- *Double triggered Phase accumulator*: the Double Phase Accumulator is given in Fig.6, with size of 16bits. It corresponds to an adder activated if $Enable = 1$ and either rising or falling clock edge is applied according to the frequency control word. In order to correct the phase, an initial input phase is used.

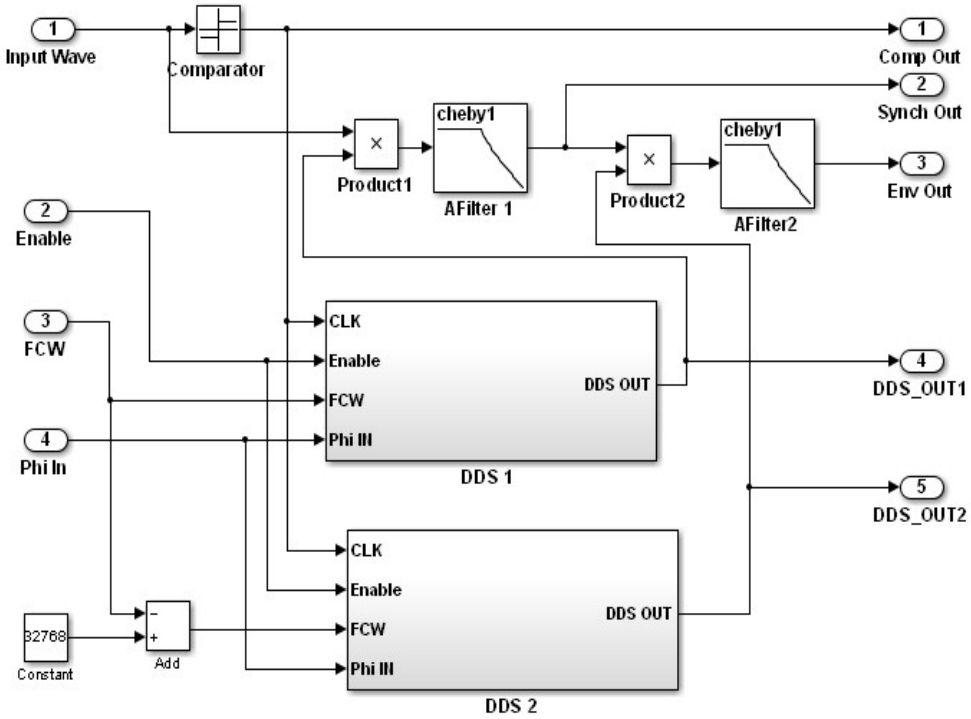

Figure 5. Simulink model for Evaluation of the proposed Coherent measurement circuit

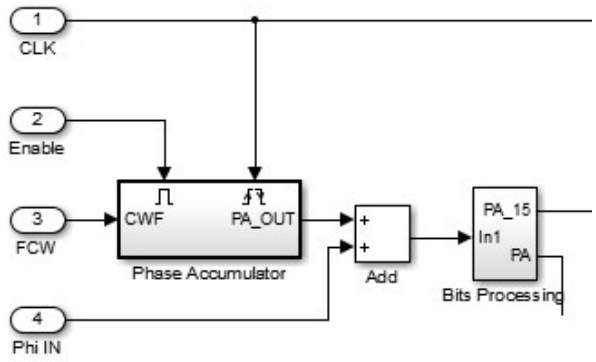

Figure 6. Double triggered Phase accumulator with offset phase.

- *DDS units:* Direct Digital Synthesis Unit computes the sine wave of frequency control word and outputs analog value DDS_OUT. As the conventional architecture, it contains the previous Double Phase Accumulator, waveform ROM and low-pass filter.

- *Analog structure 1:* it is composed of two blocks (product1, AFilter1: Chebychev 8th order, 0.1dB ripple, bandwidth: 500KHz), it allows the production of a low frequency signal whose value is controlled by the frequency control word and contains the same envelope of input wave.

- *Analog structure 2:* it is composed of two blocks (product2, AFilter2: Chebychev 8th order, 0.1dB ripple, bandwidth: 10KHz), it produces the envelope of input wave in the bandwidth of the analog low-pass filter.

3.2. Simulation results

Now, we will illustrate the evolution of different signals according to the following parameters: input wave with central frequency 1MHz, envelope: 1V-Sweep frequency in the range [0Hz -100Hz]; FCW=30000. Simulation results are plotted in the following figures:

- Fig. 7 illustrates the evolution of input wave, comparator OUT, DDS OUT and synchronized low frequency. We notice that the synchronized signal has the low value corresponding to $1MHz - \frac{2\times30000}{2^{16}}MHz = 84{,}473KHz$.

- Fig. 8 shows the input and the measured envelopes.

- Fig. 9 presents the input wave and the measured envelope.

Based on the obtained simulations results, we can deduce that the design architecture and the measurement technique ensure the coherent detection of envelope in spite of the change of the input wave frequency.

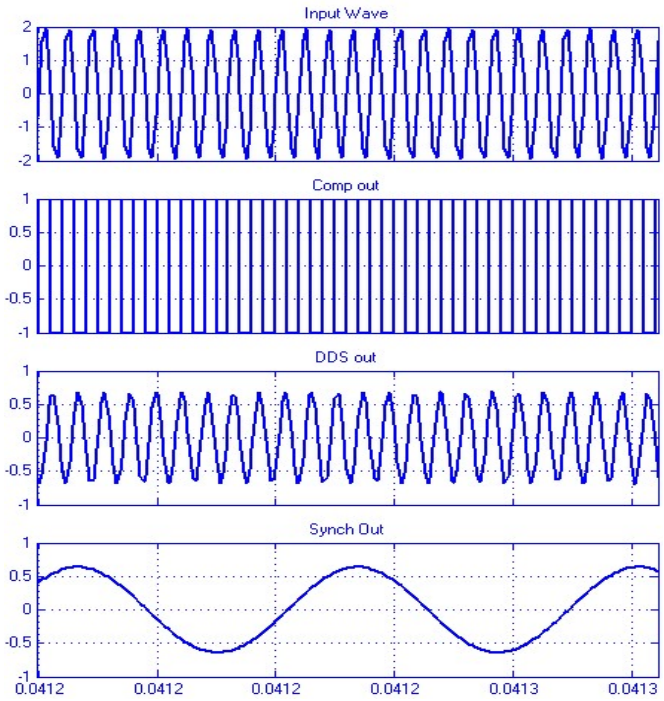

Figure 7. Input and DDS output waves

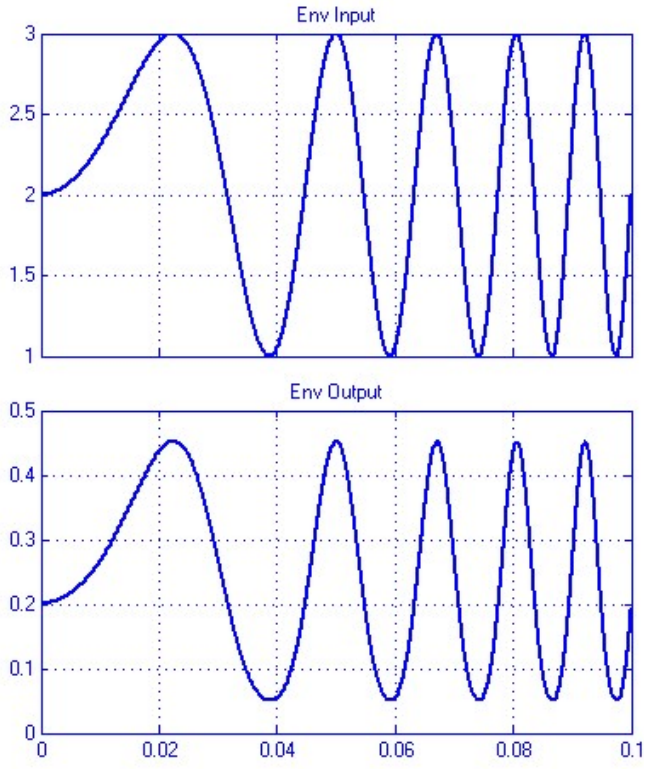

Figure 8. Input and reconstructed envelopes.

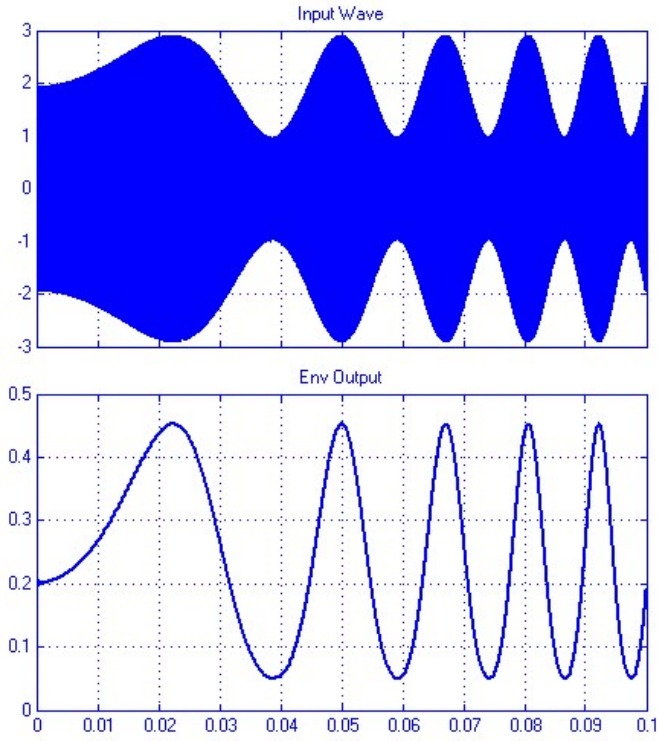

Figure 9. Input wave and its reconstructed envelope

4. Experimental Results

In this section, we will present the experimental results of DDS system and its associated measurement block. For this purpose, we have used two DDS function generators (HM 8134-3 and HM 8131-2), two analog multipliers MLT04, and two low-pass filters. Fig.10 shows the experimental Kit.

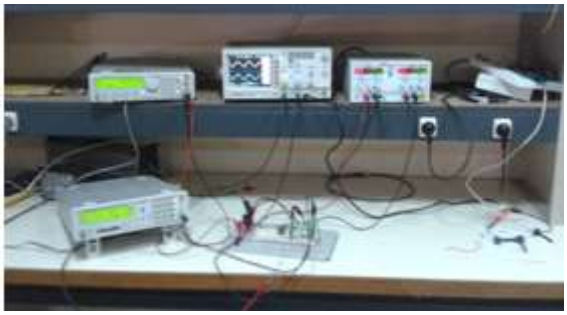

Figure 10. Experimental kit for envelope measurement and validation.

The operating parameters and measurement signals are summarized below:

- Fig. 11 presents the input signal (CH1): 1MHz - 1Vpp, and synthesized reference coherent signal (CH2): 995KHz - 4Vpp.

- Fig. 12 shows the outputs of multiplier (CH2) and low-pass filter (CH1). We measure the result frequency: 5 KHz of low frequency signal containing the constant envelope of input signal.

- Fig. 13 presents the input measurement signal (CH1): 1MHz - 1Vpp, and synthesized reference coherent signal (CH2): 999KHz – 4Vpp.

- Fig. 14 presents the outputs of multiplier (CH1) and low-pass filter (CH2). We measure the result frequency: 1 KHz of low frequency signal containing the constant envelope of input signal.

- Fig. 15 shows the sweep input signal (CH2) in the range [1MHz – 1,001MHz] and the desired output of low-pass filter (CH1) with constant synthesized signal: 999 KHz. In this case, the frequency of output signal is not constant because the DDS reconstruction is not configured to follow the frequency variation of input signal.

- Fig. 16 shows the sweep input signal (CH2) in the range [1MHz – 1,001MHz] and the desired output of low-pass filter (CH1) with synthesized signal from start frequency: 999 KHz. In this case, the frequency of output signal keeps a constant value 1KHz throughout the sweep time. This experimental result is the main objective of our work, where the designed circuit provides the synchronized digital synthesis operation and consequently the generation of low frequency signal containing the same envelope of the input signal.

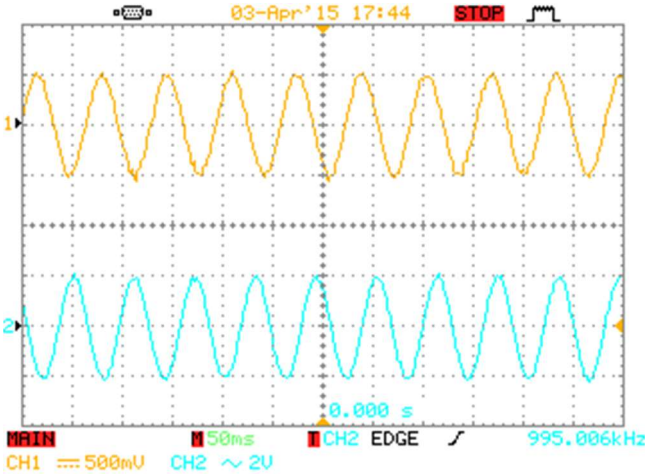

Figure 11. Input (CH1-1MHz) and synthesized reference signal (CH2-995KH);

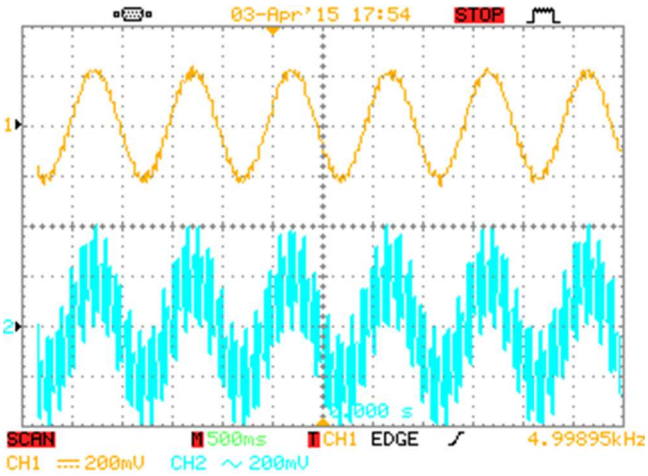

Figure 12. Filter (CH1) and multiplier (CH2) outputs for 1MHz-995KHz signals.

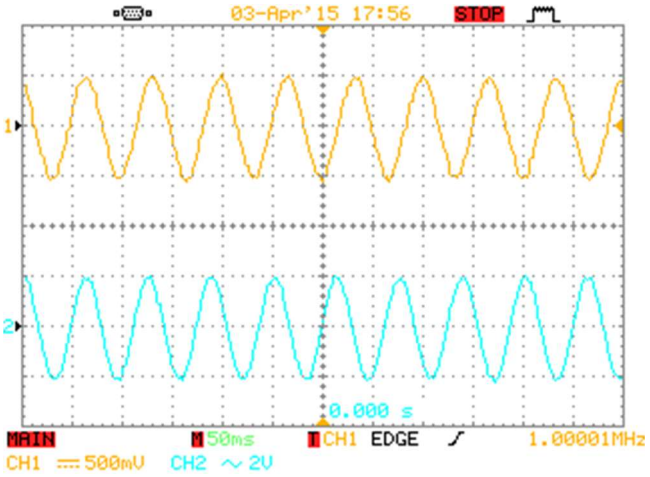

Figure 13. Input (CH1-1MHz) and synthesized signals (CH2-999KHz);

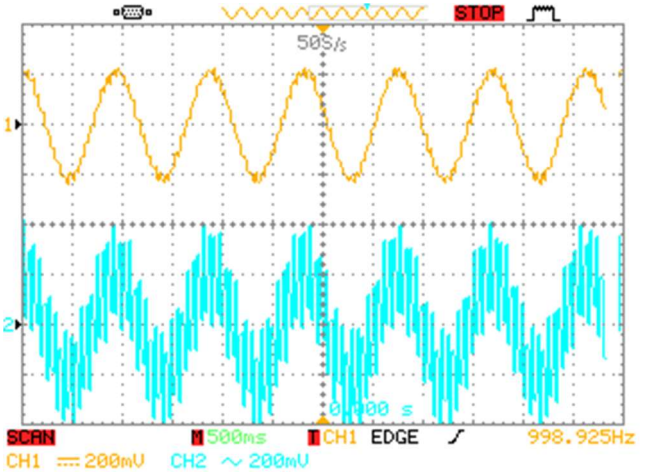

Figure 14. Filter (CH1) and multiplier (CH2) outputs for 1MHz-999KHz signals.

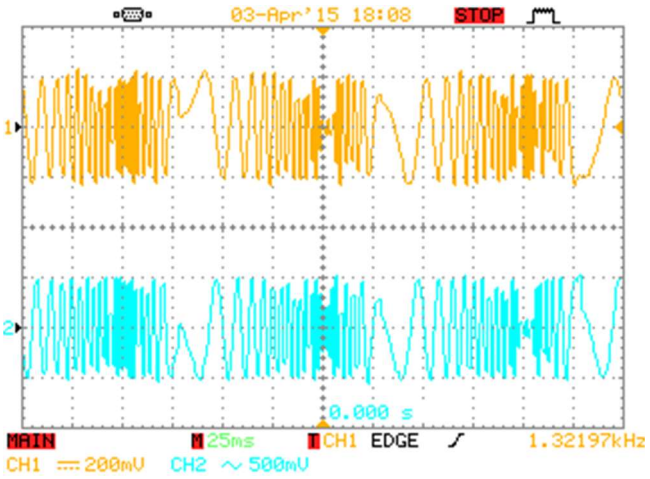

Figure 15. Input sweep [1MHz – 1,001MHz] (CH1) and filter output without synchronization (CH2).

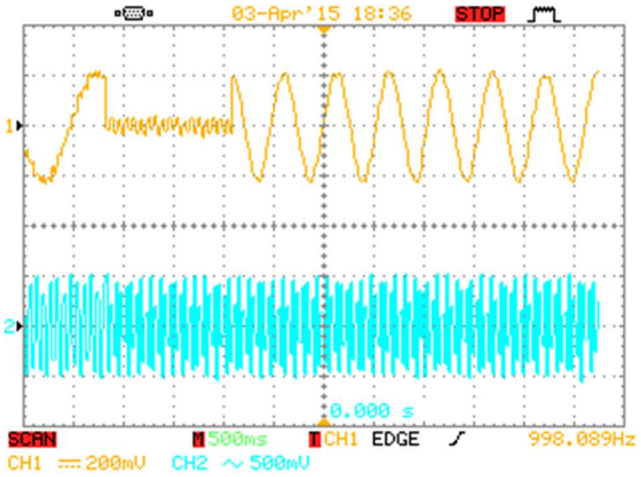

Figure 16. Input sweep input [1MHz – 1,001MHz] (CH1) and filter output with synchronization (CH2).

5. Conclusion

In this paper, we have presented the architecture of an electronic measurement circuit. This proposed circuit aims to measure the envelope of high frequency wave by coherent translation to low frequency signal that contains the same envelope. Hence, the measurement performances such as precision and resolution can be improved in the small operating frequency range. The simulation and experimental results have demonstrated the effectiveness of this circuit to measure the envelope of any input wave using DDS blocks in coherent mode. For application, we are working to implement this circuit on PSoC chip and apply it to identify the electrical impedance of crystal quartz sensors.

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