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Original Research Paper

Current-Mode Rail-to Rail Instrumentation Amplifier for General Purpose Instrumentation Applications

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Abstract: Instrumentation amplifiers are used extensively in bio-potential reading, industrial sensor applications, Wheatstone bridge amplifiers etc. In this work, a high input common-mode range instrumentation amplifier is presented. The amplifier is composed of two second generation current conveyors (CCII+) with common-mode input range close to supply swings and a differential difference current conveyor (DDCC) at the second stage with high voltage swing at the output. Also an optional DC servo loop is employed as a feedback to second stage for the removal of any possible DC offset voltage at the output which can be used for AC coupled applications. The simple design strategy with high input common-mode range and nearly rail-to-rail output stage together with increased bandwidth advantage of current-mode approach makes the proposed implementation desirable for many of the general purpose instrumentation applications. The design is made using 0.35µm AMS technology with 3V supply voltage. The operation is verified by HSPICE simulations.

Keywords: *Current-mode circuits, biomedical instrumentation, current-conveyors, current-mode instrumentation amplifier (CMIA).*

1. Introduction

Instrumentation amplifiers are extensively used for engineering applications to amplify small differential signals. The key property of these amplifiers is the ability to reject undesired common mode voltages [1]. Therefore, Common-Mode Rejection Ratio (CMRR) is the key parameter to measure the quality of an instrumentation amplifier. Generally, voltage-mode instrument amplifiers are employed in many of the engineering applications. Especially three op-amp instrumentation amplifier is the most popular structure among instrument amplifier topologies. [1-2]. However, CMRR is directly dependent on resistor matching in three op-amp configuration. Moreover, voltage-mode amplifiers are limited by gain band-width product, i.e., as the gain increases, frequency band-width decreases. An alternative is to use current-mode circuits where CMRR is not directly dependent on resistor matching. In addition, bandwidth is not directly limited by gain in current-mode instrumentation amplifiers [3, 10-11]. The first proposed configuration of Current-Mode Instrumentation Amplifier (CMIA) implementation [4] is depicted in Fig. 1. Idealized CCII+ equations are:

$$I_Y = 0 \tag{1.a}$$

$$V_X = V_Y \tag{1.b}$$

$$I_Z = I_X \tag{1.c}$$

The design is made using two of the second generation current conveyors of plus type (CCII+). In the circuit, node Y is high impedance node where the input voltage is copied to low impedance node X. In the circuit of Fig. 1, differential input voltages at node Y of both conveyors are replicated at nodes X. The voltage difference of the two of the X nodes results as current at nodes of X. Then, the current flowing through X nodes is copied to node Z at the output. Therefore the voltage at Z node is amplified by the ratio of the gain resistors of the circuit. Basic gain formula (assuming idealized components) of the CMIA shown in Fig. 1 is:

$$V_{OUT} = \frac{R_1}{R_2}(V_{in+} - V_{in-}) \tag{2}$$

The advantage of the circuit in Fig. 1 is its simplicity, high CMRR without resistor matching and wide band-width. Although CMIA in Fig. 1 gives good performance without resistor matching requirements, improved configurations are proposed utilizing both outputs of the current conveyors [2, 5- 7].

In this paper, two of the CCII+ elements with high input common-mode range with high output swing close to rail-to-rail swing is employed at the input stage. Then, another current conveyor, i.e. Differential Difference Current Conveyor (DDCC) is used at the second stage. So that higher CMRR performance and gain is possible. DDCC element is a rather new current conveyor element providing a variety of algebraic operations over the input ports [8]. By employing DDCC element at the second stage, variety of operations is possible which is advantageous for alternative implementations of instrumentation amplifiers. The circuit equation of the idealized DDCC element in matrix form is as follows:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{bmatrix} \tag{3}$$

By employing DDCC element at the second stage, variety of algebraic equations is handled easily. Moreover, an optional DC servo loop is designed for the removal of potential offset at the output which is desirable for the AC coupled instrumentation requirements. Removal of the offset voltages is crucial for the bio-potential amplifiers. The reason is that, there usually exist electrode offset at the bio-potential amplifier inputs that saturates the amplifier and only offset voltage is observed at the output of the amplifier if there is no DC removal path available.

In the next section, the structure of the design together with internal structure will be explained.

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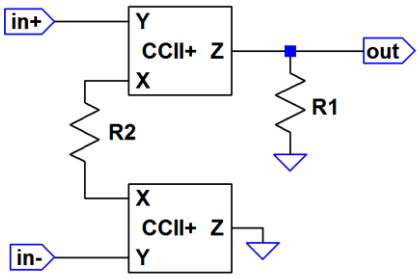

Figure 1.CCII+ based CMIA

2. CMIA Structure

The structure of the proposed instrumentation amplifier is shown in Fig. 2. Two-stage amplification scheme is suitable for higher gain for the instrumentation implementation. The first stage of the amplifier is implemented using rail-to-rail CCII+ elements. The first stage implementation is critical for high CMRR which will be explained in next section. At the second stage, the difference operation of the dual outputs of the first stage is handled using DDCC element. Moreover, integration of the output is feedback from the output to the third terminal of the DDCC. The gain formulation of the system is given as:

$$V_{X(DDCC)} = V_{Y1} - V_{Y2} + V_{Y3} \quad (4.a)$$

$$I_{X(DDCC)} = I_{Z(DDCC)} = \frac{1}{R_3}(V_{Y1} - V_{Y2} + V_{Y3}) \quad (4.b)$$

$$V_{OUT} = \frac{R_4}{R_3}(V_{Y1} - V_{Y2} + V_{Y3}), \quad (4.c)$$

$$V_{Y1} = \frac{R_1}{R_2}(V_{in+} - V_{in-}), \quad (4.d)$$

$$V_{Y2} = -\frac{R_1}{R_2}(V_{in+} - V_{in-}), \quad (4.e)$$

$$V_{Y3} = -\frac{1}{R_4 C_1}\int V_{OUT}\,dt \quad (4.f)$$

Then output of the CMIA is,

$$V_{OUT} = \frac{R_4}{R_3}\left[\frac{2R_1}{R_2}(V_{in+} - V_{in-}) + \left(-\frac{1}{R_3 C_1}\int V_{OUT}\,dt\right)\right]. \quad (5)$$

The integrator loop in the structure removes DC offset available at the output of the system. If the integrator loop is active, high pass cut-off frequency is:

$$f_{HP} = \frac{1}{2\pi\tau} = \frac{1}{2\pi R_3 C_1}. \quad (6)$$

If the offset cancellation loop is not employed, i.e. node Y3 of the DDCC is connected to GND, the gain formulation is equal to:

$$V_{OUT} = \frac{R_4}{R_3}\left[\frac{2R_1}{R_2}(V_{in+} - V_{in-})\right]. \quad (7)$$

3. Internal Building Blocks

The CMIA is built using CCII+ and DDCC elements. CCII+ elements are redesigned for rail-to-rail operation using a novel output biasing structure. DDCC element is also designed for rail-to-rail output swing together with precision output current mirrors to make the component operate close to idealized voltage and current equations. Basic operation principle of the CCII+ element is shown in Fig. 3. The circuit is composed of two differential blocks composed of PMOS input stage and NMOS input stage. Therefore the circuit is functional up to rail-to-rail swing. Differential blocks works as unity gain buffer cells to copy the input voltage at Y node to X node. The output transistors are biased using an output biasing circuit. Whenever any of the differential blocks is inactive, output biasing circuit still provides sufficient current drive for the output transistors M_{OP} and M_{ON}. Then, current at node X copied to the Z node by class AB current mirrors. The output biasing scheme for the X node output is simple so that, supply voltage is divided between the gate-to-source voltages of the four transistors as:

$$V_{SG\_OP} + V_{SG\_D1} + V_{GS\_D2} + V_{GS\_ON} = V_{DD} - V_{SS} \quad (8)$$

Since $V_{DD} - V_{SS}$ is 3V, there is sufficient voltage headroom for each of the transistor to operate properly. If the bias circuit does not exist in the structure, whenever one of the driving operational trans-conductance amplifiers (OTA) are in the off state, related output transistor M_{ON} or M_{OP} gate input floats and there exists extreme current consumption at the output stage. Using the proposed scheme, both of the output transistors are active for the full swing and provide class AB operation properly. Adjustment of the output biasing can be done by sizing of the diode connected transistors M_{D1} and M_{D2}. Selecting larger length (L) for the diode connected transistors limits the output biasing current which is important for low-power operation. Self-biasing

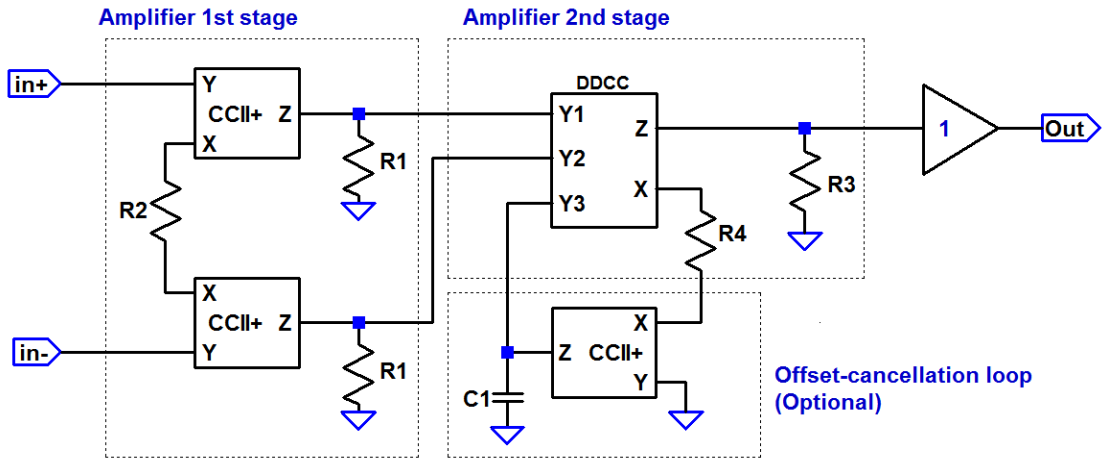

Figure 2. Circuit implementation of the proposed CMIA using CCII+ and DDCC elements

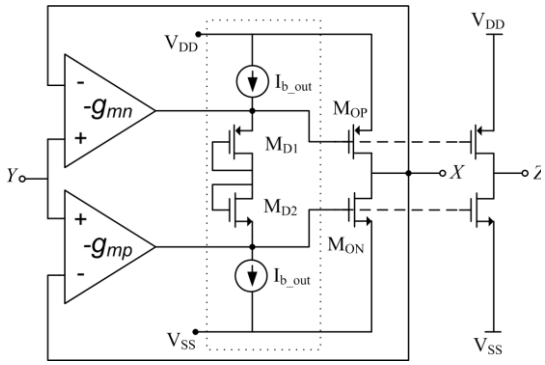

Figure 3.CCII+ working principle

scheme for driving of OTAs and output stages provides stable operation over large temperature range. Whenever bias currents of OTAs increase by temperature, bias currents I_{b_out} also increase, then quiescent drain currents (I_D) of M_{ON} and M_{OD} is limited. So that low power operation is provided over a large temperature range. Full circuit diagram with self-biasing scheme is shown in Fig. 4. Miller compensation is also employed between node X to drain of M_8 and node X to drain of M_4 is also employed.

Table 1. Transistor aspect ratios for the circuit of Fig. 4

Transistor	***W/L (μm/ μm)***
M_1 - M_2	40/2
M_3 - M_4, M_7 – M_8	20/2
M_5 - M_6	40/4
M_{OP1} – M_{OP2}	30/2
M_{ON1} – M_{ON2}	20/2
M_{B1}, M_{B4}	10/2
M_{B2}, M_{B3}	3/3
M_{B5}, M_{B6}, M_{B7}, M_{B10}	40/2
M_{B8}, M_{B9}	7/2

As explained before, the proposed instrumentation amplifier is composed of two amplifier stages. First stage of the CMIA is based on the basic structure shown in Fig. 1. Second stage is also a differential amplifier constructed using DDCC element. DDCC element is a rather new current conveyor, providing wide variety of algebraic operations. However, DDCC element has lower common-mode range. Since common-mode voltage is mostly removed at the first stage, only residual common-mode voltage appears at the second stage. So that, DDCC element can be effectively employed at the second stage. Moreover, various input algebraic operations provide also an optional DC removal input at node Y3 as shown in Fig. 2. DC removal procedure is important especially for bio-potential recordings since a low-offset voltage at the input saturates the instrumentation amplifier and prevents proper operation. So that after pre-amplification at first stage, remaining DC offset is removed using an integrator feedback loop, i.e. DC servo loop. The current-mode integrator provides grounded capacitor implementation for the integrator, which is advantageous for various implementations such as capacitance multiplication for large capacitance values, etc. The integrator is employed using a CCII+ with a capacitor shown as C1 in Fig. 2. Filter high-pass cut-off frequency can be calculated using (5).

The internal structure of the DDCC element is shown in Fig. 5. The DDCC element is based on two equivalent differential input stage, one output stage with feedback for the output X and current copying circuit from X to Z to generate Z output. The circuit is the improved version of the DDCC proposed in [8]. The aspect ratios of the circuit are given in Table 2. In the second stage of the CMIA, i.e. DDCC circuit, a rail-to-rail input is not required since large common-mode voltage component is removed at the first stage. Here, low-voltage cascode output is employed at Z node, so that rail-to-rail output is possible with high precision the output of the proposed CMIA. Current source I_b is set to 2μA with cascode current sources in the circuit. Moreover, the circuit is operational under wide variety of current values. Bias voltages V_{bias1} and V_{bias2} are set to V_{DD}-1V and V_{SS}+1V, respectively. In the proposed scenario, desired gain is possible by adjusting the R3 and R4 resistances if R1 and R2 are internally adjusted to a constant value in Fig. 2 and using (6). DC servo loop can also be de-activated by connecting Y3 input to GND. Since X node of the DDCC is constructed using voltage followers and Z node is implemented using cascade stages, output gain can be precisely adjusted.

For DC coupled implementations, Y3 node can also be used for offset removal by removing the integrator and applying a voltage divider network at node Y3. So that a simple rail-to-rail input and output operation with precision gain and various configurations is possible using the proposed CMIA structure. Output can also be supplied by a unity gain amplifier.

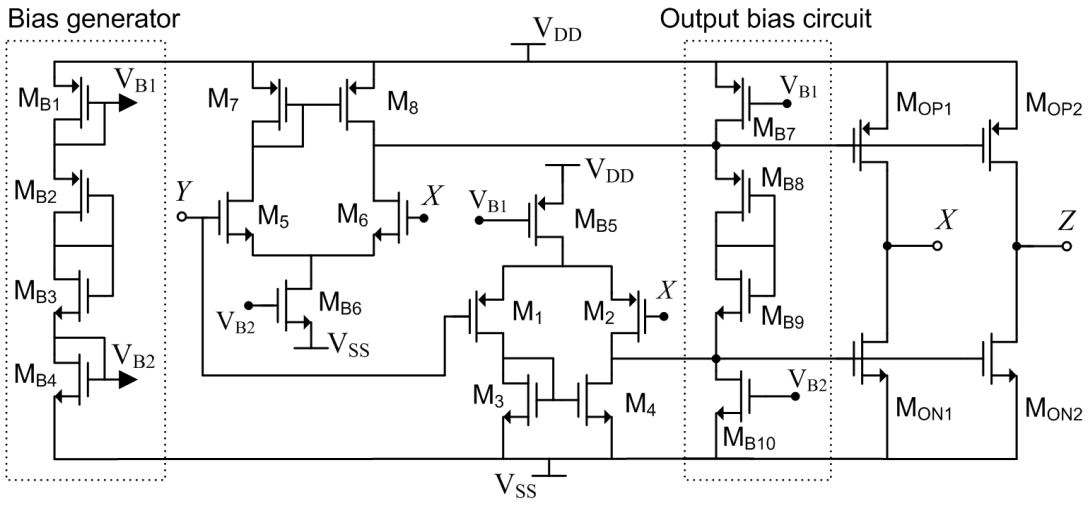

Figure 4. Circuit diagram of the CCII+

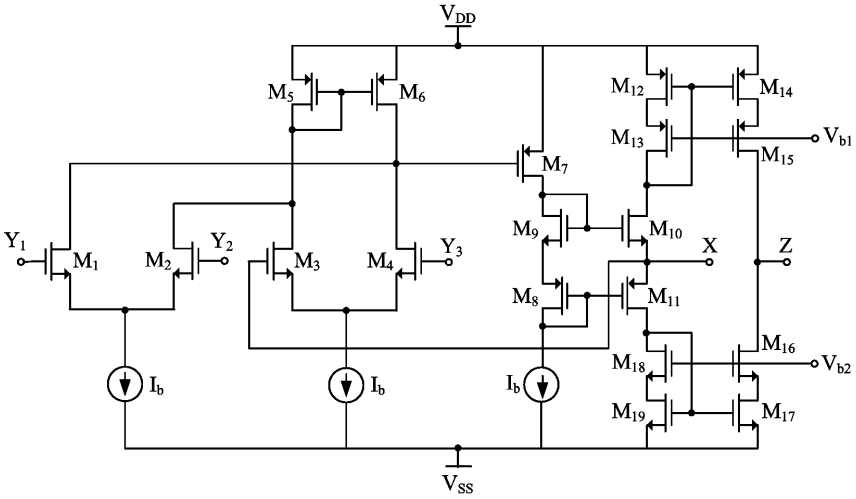

Figure 5. Internal structure of the DDCC element

Table 2. Transistor aspect ratios for the circuit of Fig. 5

Transistor	*W/L (μm/ μm)*
M_1 - M_4	40/4
M_5 – M_7	40/1
M_9 – M_{10}	20/1
M_8, M_{11}	50/1
M_{12} – M_{15}	120/1
M_{16} – M_{19}	50/1

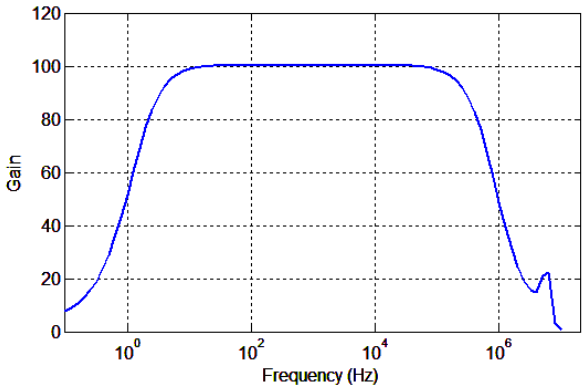

Figure 6. Frequency response of the proposed CMIA.

4. Simulation Results and Discussions

The proposed CMIA is configured for 40 dB gain. The first stage gain is selected to be 20, the second stage gain is set to 5. Using (7), R1 and R2 are selected to be 5kΩ and 500Ω, respectively. However, X nodes of the CCIIs have non-zero resistive input impedance. Due to input resistance of X nodes, using simulations, R2 is replaced by 485Ω. As a result the X node resistance of each CCII+ is estimated as (500-485) Ω /2 = 7.5 Ω. Second stage X and Z nodes of the DDCC element are close to ideal, since better output stage is designed for the DDCC element. For the second stage, R3 and R4 are selected as 100kΩ and 500kΩ, respectively. Capacitor C1 is selected as 1μF. Using (5) high-pass frequency for DC removal is 1.5 Hz, which is suitable for electro-cardiography (ECG) signals. The frequency response of the amplifier is shown in Fig. 6. The gain of 100 with cut-off frequency of 1.5 Hz is achieved using the given component values.

The CMRR performance of the proposed differential amplifier is dependent on two main design issues. One is dependent on device sizing; the other is related to device mismatch effects. CMRR related to device sizing do not have main impact when differential design strategy is selected [10]. Sizing effects mostly cancels out in the proposed structure, since differential design strategy cancels out common-mode effects two of the differential inputs applied to Y1 and Y2 nodes of the DDCC input at the second stage as the outputs from the CCII+ elements are subtracted using the second stage amplifier. If mismatch effect is not included the CMRR of the proposed structure is as high as 150 dB which is not possible in reality. By applying geometry mismatch to the differential stages of the CCII+ elements in the simulations, the CMRR is recorded as 105 dB. Therefore, matching is very critical for the pairs of M1-M2; M3-M4; M5-M6; and, M7-M8 of Fig. 4. CMRR calculation in [13, 14] also shows that if two of the differential inputs have same gain error, the common-mode effect is minimized.

Larger L values are employed for the transistors at the first stage of the CCII+ in Fig. 4, NMOS transistor lengths especially kept larger to reduce flicker noise at the first stage. As a result, 850 nV/√Hz input referred noise at 1 Hz is recorded. Noise level is reduced at higher frequencies, as expected. The results are summarized in Table 1. The CMRR recording of the propsed CMIA is comparable with the implementations in [14-16].

Table 3. Design Summary

Technology	0.35μm
Supply	3 V
Bandwidth	550kHz
Gain	40 dB (adjustable)
CMRR	105 dB
Input noise @ 1Hz	850 nV/√Hz
Input&Output Swing	0.1V – 2.9V
Power Consumption	300μW

5. Conclusion

In this paper, a rail-to-rail CMIA circuit is designed. The circuit is designed for general purpose needs and suitable for bio-potential amplification, industrial sensor conditioning etc. The CMIA is based on two amplifier stages and DC off-set removal is possible for AC coupled implementations. The design has high CMRR, and low input referred noise compared to amplifiers without chopper stabilization. Simplicity of the design procedure with rail-to-rail operation and easy implementation of DC offset removal are the advantages of the proposed CMIA.

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