

Performance Evaluation of Multi-carrier PWM Techniques: PD, POD and APOD

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Abstract: In industrial applications, modulation strategies play a significant role to provide the effective voltage generation at the outputs of inverter structures. Also, the modulation strategies are important to generate output voltages with lower harmonic distortions. For this purpose, there are several modulation techniques to produce stepped voltage waveforms by reducing harmonics for high voltage levels. Therefore, this work introduces the comparative study of multi-carrier based pulse width modulation (PWM) methods used in high power rated inverters. In this regard, phase disposition (PD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD) PWM strategies are tested in five-level cascaded H-bridge inverter. The performance consequences are received for different carrier frequencies, and total harmonic distortions are evaluated for tested methods. The results show that total harmonic distortion in APOD-PWM controlled inverter is less than other methods. In addition, total harmonic distortion values are performed for frequency values, which are from 0.5 kHz to 4 kHz.

Keywords: Multi-carrier PWM, Phase Disposition, Phase Opposition Disposition, Alternative Phase Opposition Disposition

1. Introduction

In industrial applications, inverters are known as power electronic converters which convert dc electrical power into ac electrical power. These converters exist in different implementations such as renewable energy integration, custom power devices, industrial and home appliances in different power ranges [1, 2]. In order to convert dc power into ac power, traditional inverters cause high switching losses, electromagnetic interferences and high total harmonic distortion (THD) [3]. An alternative solution is the utilization of multilevel inverter to minimize the disadvantages of conventional inverters [4-6]. Among multilevel inverters, cascaded H-bridge inverters have high-efficiency conversion ratio, low electromagnetic interferences and low power losses in energy conversion implementations compared to conventional inverters [7]. Because they have more smooth voltage waveforms with an increased number of voltage levels compared to classical inverters. Besides, they require low-rated filters thereby diminishing the entire system dimension. These inverters also reduce the THD level at output voltage thus increasing the power quality of the whole system [7, 8].

In order to generate voltage levels in the inverters, there are a number of modulation strategies. They can be categorized as square wave pulse-width modulation (PWM), hysteresis controller, space vector and carrier PWM structures [9, 10]. Among these strategies, carrier PWM is more compact and simpler compared to other PWM methods. Besides, multi-carrier PWM approaches are improved to switch the solid-state devices for cascaded H-bridge inverters [11]. There are various multi-carrier PWM strategies which are defined as subcategories. The most well-known multi-carrier PWM strategies are Phase Disposition

(PD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD) [11, 12].

In the scope of the study, the analysis and consequences of five-level cascaded H-bridge inverter are tested for various multicarrier PWM strategies. The control strategies and performances of used methods are introduced in detail.

2. Cascaded H-Bridge Inverter

The cascaded H-bridge dc-ac converters have attracted great attention in high power ratings due to the requirement of medium voltage inverters. These converters consist of poly buildings of single-phase H-bridge modules [13]. These modules are traditionally tied in the cascaded structure at the load-side for the generation of high voltages and decrease harmonic distortions. The cascaded inverters need independent dc voltage sources which supply different H-bridge modules [14, 15]. According to the bipolar modulation strategy, S1- S4 are simultaneous and used to +Vdc when they are turned on [16].

The organization of a single phase H-bridge module is presented in Figure 1. The structure consists of two separate legs based on two switches for each leg [17]. The input dc voltage is fixed and equal to Vdc while the output voltage is named as Vo. With switching combinations of S1-S4, three voltage levels are originated at the output of inverter: +Vdc, 0, -Vdc [18]. In the operation of the inverter, S1-S4 and S2-S3 are turned on to generate Vdc and -Vdc levels, respectively [16]. The equivalent circuits of inverter during switching states are introduced in Fig. 2. The switching states to generate all voltage levels are also given. In the first state, S1 and S4 are triggered and the output voltage is equal to +Vdc [18]. In this state, the current follows the path from S1 and returns from S4. In the second stage, S2 and S3 are switched and the output voltage is obtained as the inverse voltage of the dc source. This is the negative cycle operation of conventional H-bridge inverter. In state 3, all switches are turned off to obtain zero value at the load voltage [18, 19].

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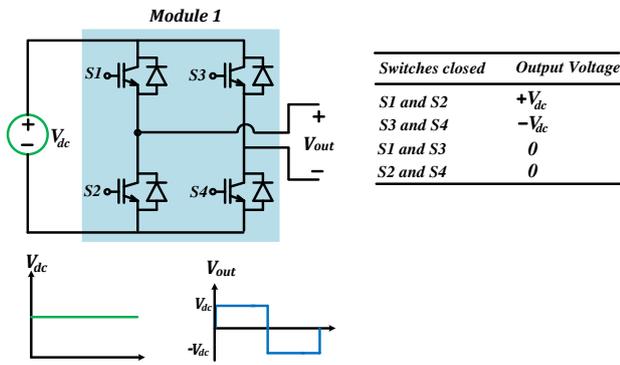


Fig. 1. The scheme of a single H-bridge module

The scheme of cascaded H-bridge inverter is introduced in Figure 2. In the construction, the outputs of each H-bridge modules are tied in series to create higher voltage levels of cascaded H-bridge inverter [17, 20, 21]. The value of load voltage is the accumulation of output voltages in each module [22]. According to the numbers of H-bridge modules, the voltage levels are described below [15, 23]:

$$N = 2m + 1 \quad (1)$$

Where N is voltage level and m is the number of modules.

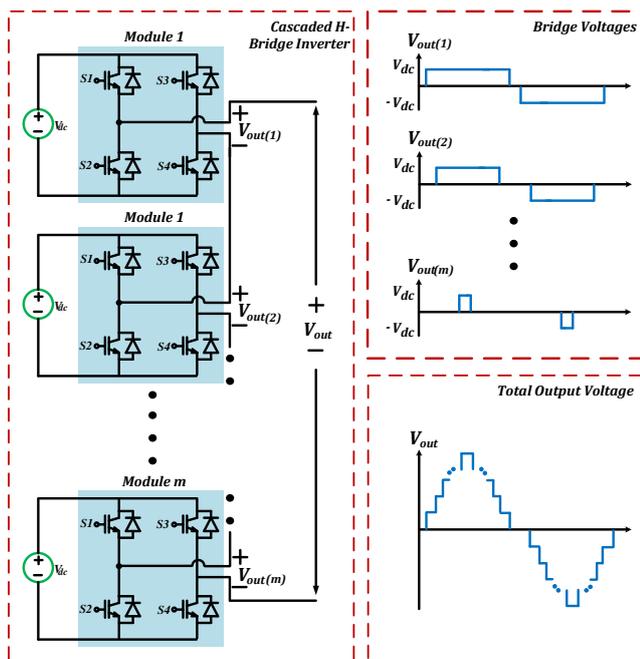


Fig. 2. The arrangement of n-level cascaded inverter

In a cascaded structure, the utilization of two separate H-bridge modules generates five voltage levels at the load-side. For higher values, the load voltage is the aggregation of each module and it is expressed below [24]:

$$V_o = V_{o1} + V_{o2} + V_{o3} + \dots + V_{o(m-1)} + V_{o(m)} \quad (2)$$

The Fourier series of the load voltage for n-module consists of only odd-order harmonics and it is defined as [15, 18]:

$$V_o(t) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5,7,\dots}^{\infty} [\cos(n\alpha_1) + \cos(n\alpha_2) + \dots + \cos(n\alpha_k)] \frac{\sin(n\omega_o t)}{n} \quad (3)$$

The coefficients of Fourier series are given:

$$V_n = \frac{4V_{dc}}{n\pi} [\cos(n\alpha_1) + \cos(n\alpha_2) + \dots + \cos(n\alpha_k)] \quad (4)$$

In which n are positive odd-numbers.

The modulation index (Mi) is equal to Vdc for n-modules [15, 17]:

$$M_i = \frac{V_1}{4kV_{dc}/\pi} = \frac{\cos(\alpha_1) + \cos(\alpha_2) + \dots + \cos(\alpha_k)}{k} \quad (5)$$

3. Multi-Carrier PWM Methods

Multi-carrier based PWM techniques are preferred for cascaded inverters and use more than one carrier which may be in the triangular or saw-tooth form [11]. The reference signal in multi-carrier PWM strategy is generally sinusoidal signal or error in the system [9, 12]. This study pays attention to the following multi-carrier PWM methods:

- PD-PWM
- POD-PWM
- POD-PWM

3.1. PD-PWM

In PDPWM strategy, a number of carriers are employed with the single reference signal. The phase information of carrier waveforms are selfsame and the carriers are arranged thereby generating coordinated voltage levels [25]. Figure 4 shows the arrangement of PDPWM for switching of five voltage levels in a cascaded inverter. It is obvious that the modulation index is equal to 1 and the frequency of carrier is 500 Hz in presentation form. Carrier 1 is used to generate switching signals of S1-S4. Carrier 2 is employed to generate switching signals of S2-S3. Carrier 3 is used to generate switching signals of S5-S8. And, Carrier 4 is performed to generate switching signals of S6-S7.

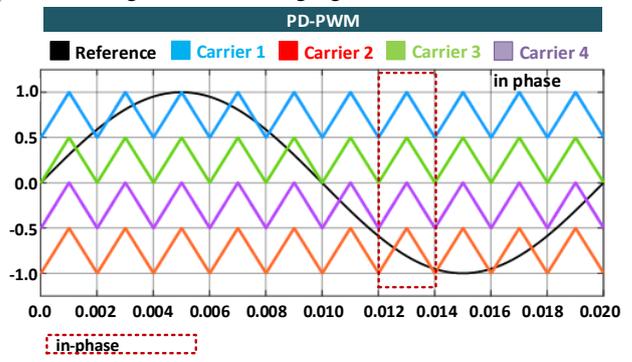


Fig. 3. The modulation strategy of PD-PWM

3.2. POD-PWM

In this technique, the carriers in positive x-axis have 180° phase difference compared to carriers in the negative side of the x-axis [26, 27]. Figure 3 presents the multi-carrier structure of POD-PWM. Carrier 1 is used to generate switching signals of S1-S4. Carrier 2 is employed to generate switching signals of S2-S3. Carrier 3 is used to generate switching signals of S5-S8. And, Carrier 4 is performed to generate switching signals of S6-S7. According to the waveform, Carrier and Carrier 4 are out of 180° phase difference [25]. The modulation index is selected as 1 and the carrier frequency is 500 Hz.

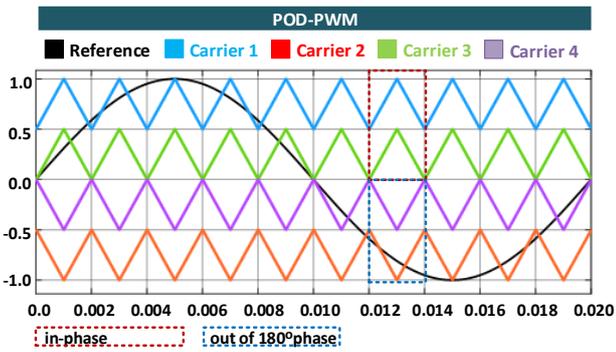


Fig. 4. The modulation strategy of POD-PWM

3.3. APOD-PWM

In APOD-PWM strategy, there are 180° phase difference between the adjacent carrier signals [27, 28]. The multi-carrier structure of APOD-PWM is given in Figure 5. In this method, Carrier 1 and carrier 4 are in phase and out of 180-degree phase compared to carrier 2 and carrier 3 [26].

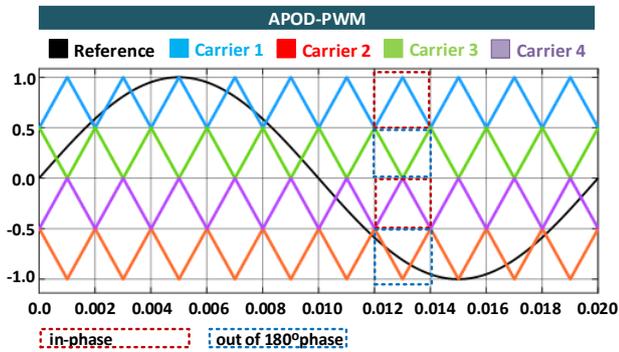


Fig. 5. The modulation strategy of APOD-PWM

4. Results & Discussion

Multicarrier PWM techniques are modeled and tested in five-level cascaded H-bridge inverter by using Simulink environment. The modeled system of multicarrier PWMs controlled inverter structure is shown in Figure 6. It is clear that the inverter consists of two H-bridge modules and generates five voltage levels at the output. The dc input voltage is equal to 100 V for each source and load consists of a resistor. The system parameters of the designed model is given in Table 1.

Table 1. System parameters

Parameter	Value
Input voltage	100 Vdc
Transistor type	MOSFET
Load	Resistor-10 ohm
Inverter power	2 kVA
Reference Signal	$\text{Sin}(314.159t+0^\circ)$
Carrier Frequency	0.5 kHz to 4 kHz
Resolution time	20 us
Harmonic order	Up to 50th component

In the performance stage, multi-carrier PWM methods are performed to generate five voltage levels in a cascaded H-bridge inverter. In this case study, the modulation index is equal to “1” and the carrier frequency is 3 kHz. In the switching process by using PD-PWM, POD-PWM and APOD-PWM, the signals of S1, S2, S3 and S4 are shown in Figure 7.

According to the switching states, five voltage levels are generated at the load-side. Figure 8 presents the voltage waveforms of output versus time. In the case study, results are obtained for 10 periods. The period value is 20 ms. It is clear that the maximum value of output voltage is equal to 200 V and the voltage step is 100 V.

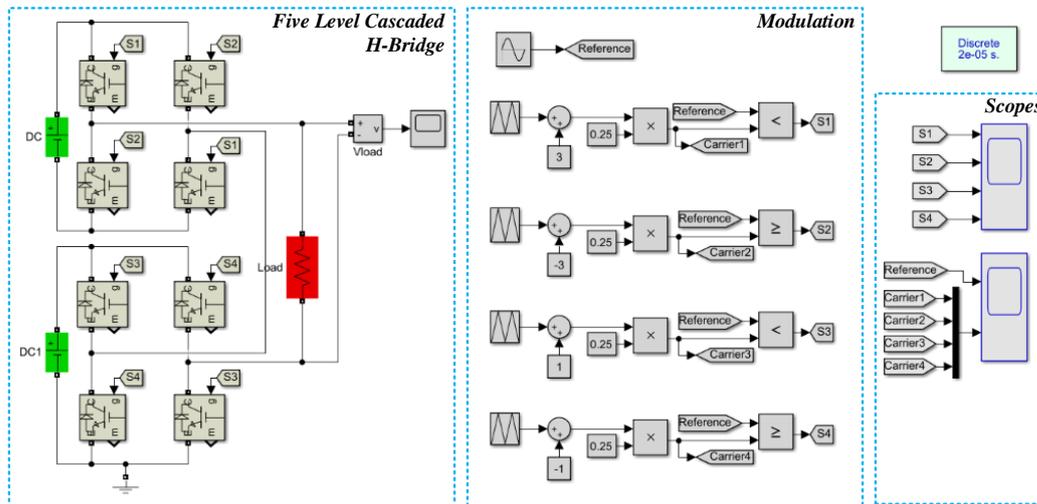


Fig. 6. The modeled system based on multi-carrier PWM strategies

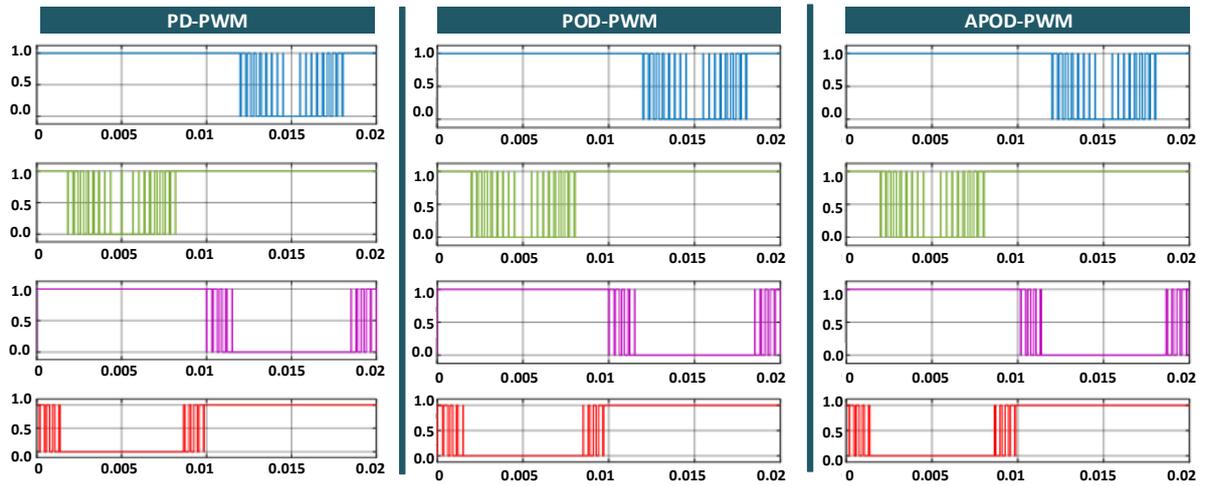


Fig. 7. The switching signals by using PD-PWM, POD-PWM and APOD-PWM (at 3 kHz)

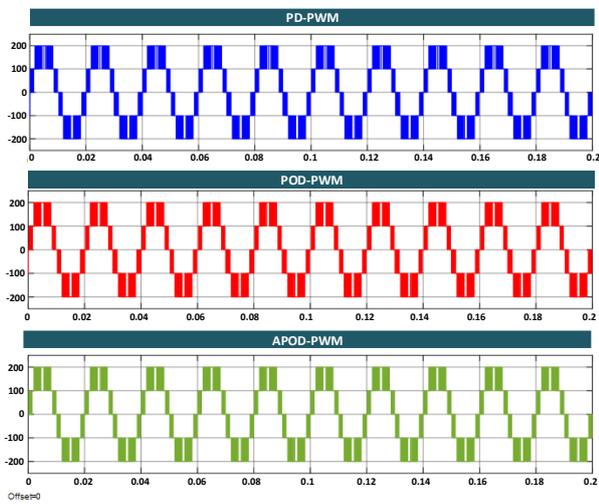


Fig. 8. Voltage waveforms versus time (at 3 kHz)

THD performances of tested multi-carrier PWM methods for output voltages are shown in Figure 9. The case is tested under 3 kHz and output filter is not used at the outputs. THD performance of PD-PWM is 5.44% while it is 3.34% for POD-PWM. However, APOD-PWM shows excellent results compared to PD-PWM and APOD-PWM. THD value is 2.25% for APOD-PWM.

The multi-carrier PWM methods are also tested for different carrier frequencies. In performance studies, carrier frequency changes from 0.5 kHz to 4 kHz. At 0.5 kHz, THD values for used methods are approximately 25%. Also, THD decreases as carrier frequency increases to higher values. It is shown that THD value is nearly 3% for all methods. All values are given in Table 2.

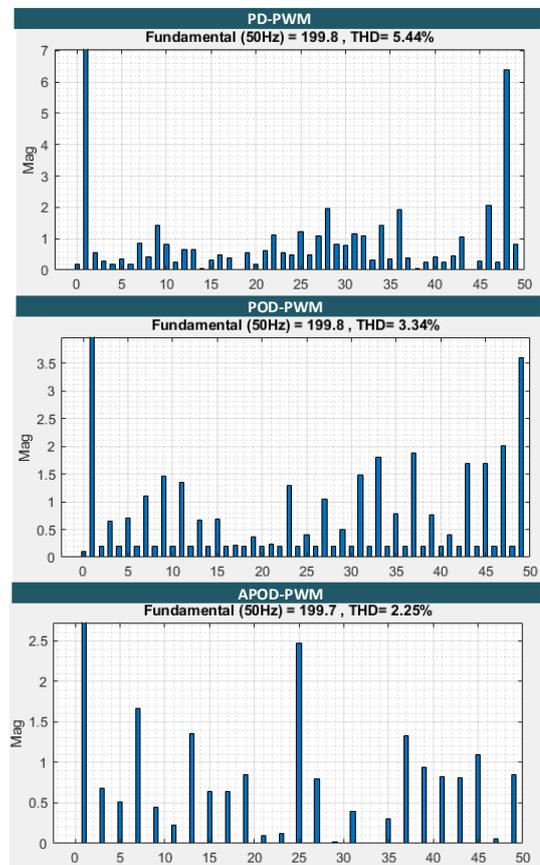


Fig. 9. THD spectrum of multicarrier PWM techniques according to the harmonic orders

Table 2. THD values for multi-carrier PWM methods for different carrier frequency values

THD Values			
Frequency	PD-PWM	POD-PWM	APOD-PWM
0.5 kHz	24,34 %	25,29 %	25,57 %
1 kHz	22,95 %	21,28 %	24,13 %
2 kHz	20,46 %	20,38 %	20,71 %
3 kHz	5,44 %	3,34 %	2,25 %
4 kHz	2,39 %	2,42 %	2,14 %

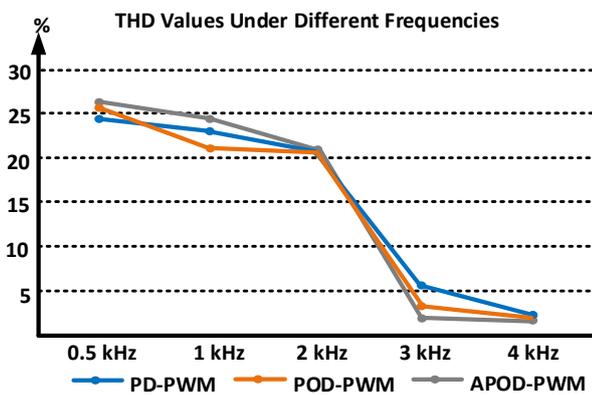


Fig. 10. THD values of PD-PWM, POD-PWM and APOD-PWM versus carrier frequency

5. Conclusion

This paper presents the performance comparison of multi-carrier PWM methods implemented in the generation of high voltage levels. PD-PWM, POD-PWM and APOD-PWM are multi-carrier PWM methods and use different carrier signals in order to generate high voltage levels at the output. For this reason, these methods are performed in five-level cascaded H-bridge inverter and performance results are given. The modulation strategies are tested and evaluated in different frequency values, which are between 0.5 kHz and 4 kHz. According to the obtained results for 3 kHz, APOD-PWM presents excellent results in comparison with PD-PWM and POD-PWM. The THD value for APOD-PWM is 2.25% and it is less than other methods. Also, THD values for different carrier frequency values are presented in the study.

References

[1] S. Mariethoz, "Systematic Design of High-Performance Hybrid Cascaded Multilevel Inverters With Active Voltage Balance and Minimum Switching Losses," *IEEE Transactions on Power Electronics*, vol. 28, no. 7, pp. 3100-3113, 2013.

[2] K. Kim, H. Cha, and H. Kim, "A New Single-Phase Switched-Coupled-Inductor DC-AC Inverter for Photovoltaic Systems," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5016-5022, 2017.

[3] D. R. Joca, L. H. S. C. Barreto, D. d. S. Oliveira, P. P. Praça, R. N. A. L. Silva, and G. A. L. Henn, "THD analysis of a modulation technique applied for THD reduction," Brazilian Power Electronics Conference, Gramado, Brazil 2013, pp. 177-182.

[4] A.-R. Haitham, M. Mariusz, and A.-H. Kamal, "Multilevel Converter/Inverter Topologies and Applications," in *Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications* ed., IEEE, 2014, pp. 832-862.

[5] W. Bin, "Cascaded H-Bridge Multilevel Inverters," in *High-Power Converters and AC Drives* ed., IEEE, 2006, pp. 450-490.

[6] V. Roberge, M. Tarbouchi, and F. Okou, "Strategies to Accelerate Harmonic Minimization in Multilevel Inverters Using a Parallel Genetic Algorithm on Graphical Processing Unit," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5087-5090, 2014.

[7] R. Gupta, A. Ghosh, and A. Joshi, "Switching Characterization of Cascaded Multilevel-Inverter-Controlled Systems," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, pp. 1047-1058, 2008.

[8] S. Amamra, K. Meghriche, A. Cherifi, and B. Francois, "Multilevel

Inverter Topology for Renewable Energy Grid Integration," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8855-8866, 2017.

[9] D. Patel, R. Saravanakumar, K. K. Ray, and R. Ramesh, "A review of various carrier based PWM methods for multilevel inverter," India International Conference on Power Electronics 2010 (IICPE2010), New Delhi, India, 2011, pp. 1-6.

[10] V. Gaikwad, S. Mutha, R. Mundhe, O. Sapar, and T. Chinchole, "Survey of PWM techniques for solar inverter," International Conference on Global Trends in Signal Processing, Information Computing and Communication (ICGTSPICC), Jalgaon, India., 2016, pp. 501-504.

[11] Y. Babkrani, A. Naddami, S. Hayani, M. Hilal, and A. Fahli, "Simulation of Cascaded H - Bridge Multilevel Inverter with Several Multicarrier Waveforms and Implemented with PD, POD and APOD Techniques," International Renewable and Sustainable Energy Conference (IRSEC), Tangier, Morocco, 2017, pp. 1-6.

[12] S. B. Student, D. Joshi, M. Singh, and R. Sharma, "Evaluation of modulation strategies for PV fed DCMLIs and its application to dynamic load," International Conference on Power, Control and Embedded Systems (ICPCES), Allahabad, India, 2014, pp. 1-6.

[13] V. Sridhar, S. Umashankar, P. Sanjeevikumar, V. K. Ramachandaramurthy, L. Mihet-Popa, and V. Fedák, "Control Architecture for Cascaded H-Bridge Inverters in Large-Scale PV Systems," *Energy Procedia*, vol. 145, pp. 549-557, 2018.

[14] H. Iman-Eini and S. B. Tennakoon, "Investigation of a cascaded H-bridge photovoltaic inverter under non-uniform insolation conditions by hardware-in-the-loop test," *International Journal of Electrical Power & Energy Systems*, vol. 105, pp. 330-340, 2019.

[15] Y. Yu, G. Konstantinou, B. Hredzak, and V. G. Agelidis, "Power Balance of Cascaded H-Bridge Multilevel Converters for Large-Scale Photovoltaic Integration," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 292-303, 2016.

[16] L. Sun, Z. Wu, F. Xiao, X. Cai, and S. Wang, "Suppression of Real Power Back Flow of Nonregenerative Cascaded H-Bridge Inverters Operating Under Faulty Conditions," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5161-5175, 2016.

[17] A. S. Gadalla, X. Yan, S. Y. Altahir, and H. Hasabelrasul, "Evaluating the capacity of power and energy balance for cascaded H-bridge multilevel inverter using different PWM techniques," *The Journal of Engineering*, vol. 2017, no. 13, pp. 1713-1718, 2017.

[18] D. Hart, "Inverters," in *Power Electronics*. vol. 1 1st ed., Mc Graw Hill, 2011, pp. 331-386.

[19] L. Zhang, K. Sun, Y. Xing, and J. Zhao, "A Family of Five-Level Dual-Buck Full-Bridge Inverters for Grid-Tied Applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7029-7042, 2016.

[20] S. Vavilapalli, S. Umashankar, P. Sanjeevikumar, V. Fedák, L. Mihet-Popa, and V. K. Ramachandaramurthy, "A Buck-Chopper Based Energy Storage System for the Cascaded H-Bridge Inverters in PV Applications," *Energy Procedia*, vol. 145, pp. 534-541, 2018.

[21] C. Kannan, N. K. Mohanty, and R. Selvarasu, "A new topology for cascaded H-bridge multilevel inverter with PI and Fuzzy control," *Energy Procedia*, vol. 117, pp. 917-926, 2017.

[22] J.-H. Lee and K.-B. Lee, "A Fault Detection Method and a Tolerance Control in a Single-Phase Cascaded H-bridge Multilevel Inverter," *IFAC-PapersOnLine*, vol. 50, no. 1, pp. 7819-7823, 2017.

[23] J. Sastry, P. Bakas, H. Kim, L. Wang, and A. Marinopoulos, "Evaluation of cascaded H-bridge inverter for utility-scale photovoltaic systems," *Renewable Energy*, vol. 69, pp. 208-218, 2014/09/01/ 2014.

[24] V. K. Gupta and R. Mahanty, "Optimized switching scheme of cascaded H-bridge multilevel inverter using PSO," *International*

Journal of Electrical Power & Energy Systems, vol. 64, pp. 699-707, 2015.

- [25] M. M. Harin, V. Vanitha, and M. Jayakumar, "Comparison of PWM Techniques for a three level Modular Multilevel Inverter," *Energy Procedia*, vol. 117, pp. 666-673, 2017.
- [26] A. António-Ferreira, C. Collados-Rodríguez, and O. Gomis-Bellmunt, "Modulation techniques applied to medium voltage modular multilevel converters for renewable energy integration: A review," *Electric Power Systems Research*, vol. 155, pp. 21-39, 2018.
- [27] W. Subsingha, "A Comparative Study of Sinusoidal PWM and Third Harmonic Injected PWM Reference Signal on Five Level Diode Clamp Inverter," *Energy Procedia*, vol. 89, pp. 137-148, 2016.
- [28] N. Susheela and P. S. Kumar, "Performance Evaluation of Carrier Based PWM Techniques for Hybrid Multilevel Inverters with Reduced Number of Components," *Energy Procedia*, vol. 117, pp. 635-642, 2017.